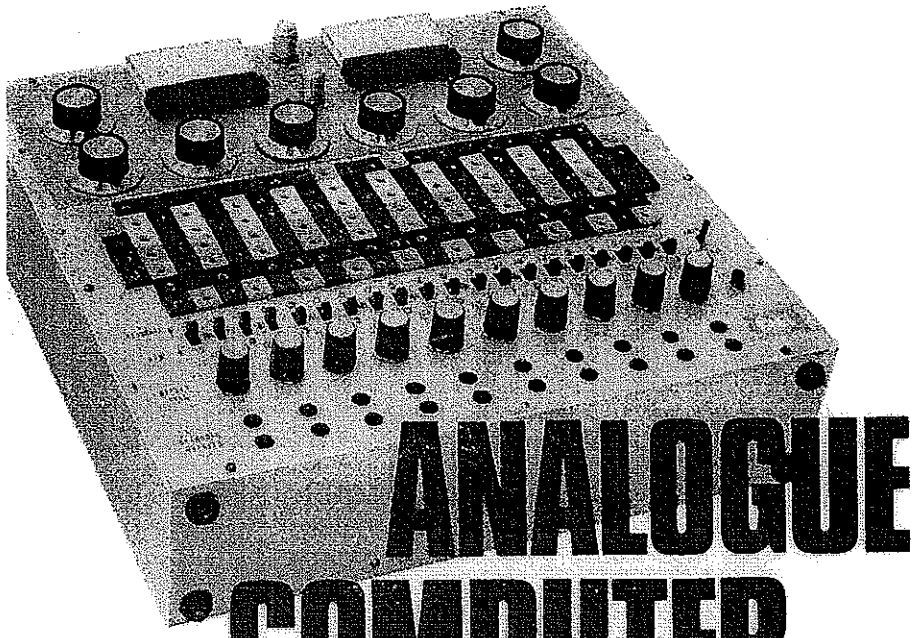


ANALOGUE COMPUTER

P. J. KRONIS B.Sc.

PART 2

HAVING formed a general picture of the workings of the analogue computer, the complete circuit of a computing element can now be described. This is shown in Fig. 2.1. The basic circuits of input and feedback, components connected around the op-amp can be readily recognised. The input comprises four resistors, R_1 to R_4, which are connected to sockets in the patch panel and to the inverting input of the op-amp, via switches RLA2, S1c, and S1b. The feedback circuit consists of R5, C1 and C2, which can be selected by means of switch S1a and sockets (C7, B6 and C6) on the patch panel.

Consider switch S1a set so that R5 is selected in the feedback loop. The computing element now becomes a summer. By recalling the equation for the addition circuit that was described last month and by substituting the values for R5, R1, R2, R3, and R4 it can be seen that a voltage applied at inputs 1 and 2 will be multiplied by unity,

$$\left(\frac{R5}{R1 \text{ or } R2}\right) = \frac{1}{1} = 1.$$

whereas inputs 3 and 4 will multiply an input voltage by 10.

$$\left(\frac{R5}{R3 \text{ or } R4}\right) = \frac{1}{0{\cdot}1} = 10.$$

With capacitor C1 selected in the feedback loop, the computing element is converted to an integrator and if values are substituted in the equation for the integrator, it can again be shown that inputs 1, 2 and 3, 4 give a gain of 1 and 10 respectively. The selection of C2 in the feedback loop increases the gain of all inputs by a factor of 10. This is usually referred to as a nose gain of 10. The symbols used to denote adders and integrators with the relevant gain values are shown in Fig. 2.2.

The "Initial Condition" resistors R6 and R7 are brought into the circuit by means of switches RLA2 and S1d. VR1 is a 10kΩ potentiometer, which provides the op-amp with external offset nulling. This is connected across pins 1 and 5, with the pot slider taken to the negative supply rail. The non-inverting input of the op-amp is grounded via R8. The value of this resistor should be chosen for good thermal drift performance. The optimum resistance would be equal to the parallel value of the input and feedback resistances. Since in this case there are two values of input resistances, a compromise solution is necessary.

The circuit of Fig. 2.1 represents just one computing element and analogue computers may have many such elements. The prototype has ten computing amplifiers which is an adequate number for the solution of fairly complex problems.

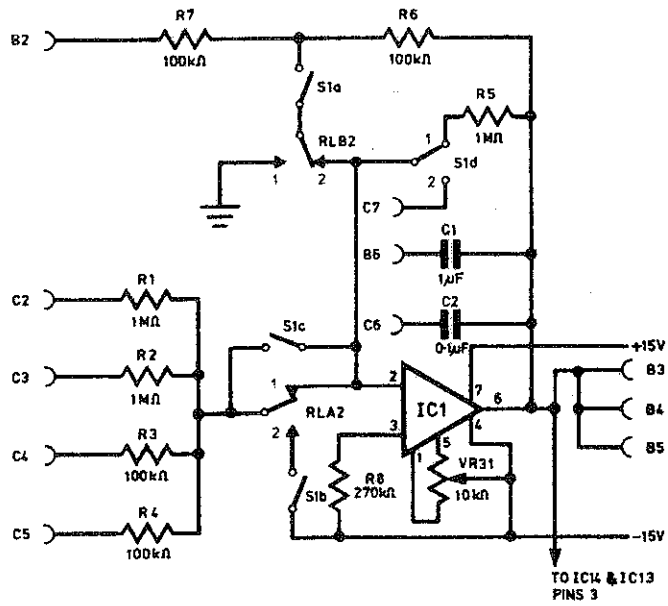


Fig. 2.1. Circuit diagram showing one of the ten computing elements of the Analogue Computer

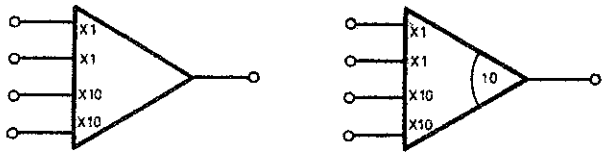


Fig. 2.2. Symbols used to denote adders and integrators

Mode Control is achieved by means of relay contacts RLA2 and RLB2. Relays are necessary because all ten amplifiers need to be controlled simultaneously. Table 1 shows the positions of relay and other switches for mode control of summers and integrators.

	SUMMER			INTEGRATOR		
SWITCH	COMPUTE	HOLD	RESET	COMPUTE	HOLD	RESET
RLA2	1	2	2	1	2	2
RLB2	1	1	2	1	1	2
S1a		OPEN			CLOSED	
S1b		OPEN			CLOSED	
S1c		CLOSED			OPEN	
S1d	1	1	1	2	2	2

TABLE 1

Fig. 2.5 shows how the ten computing amplifiers are arranged on a printed circuit board with the component overlay shown in Fig. 2.7. At the extreme ends of the board the two four-quadrant multiplier i.c.s are accommodated. This main p.c.b. is connected to other points in the computer by means of edge connectors.

The Four-Quadrant Multipliers

So far it has been shown how to multiply a variable voltage by a constant. This is easily done, using the coefficient multiplier, in conjunction with the amplifier gain. The formation of the product of two variables is much more difficult to obtain. Of the many methods that have been devised, most have involved the use of devices with certain characteristics, e.g. a diode function generator can be set up to provide a square law action, or a log-antilog action. Op-amps are usually employed with these circuits.

For the sake of simplicity and compactness it was decided to use two four-quadrant multiplier i.c.s in the prototype. As their name implies these can multiply in four quadrants,

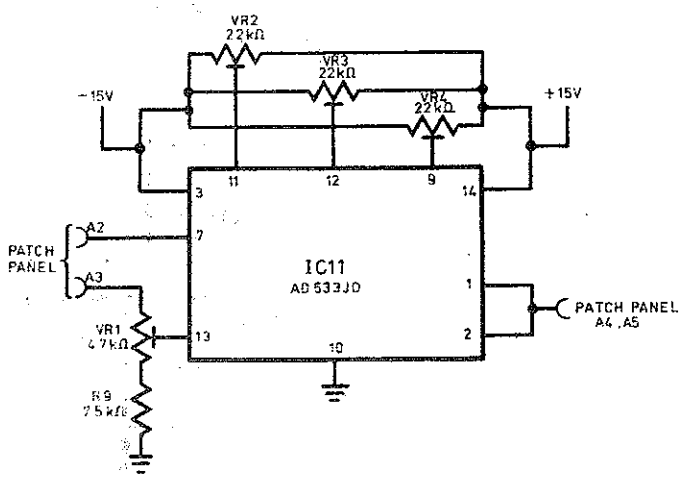


Fig. 2.3. Circuit diagram of the Four Quadrant Multiplier

which means that either or both voltages can be positive or negative. This dispenses with the need to have an absolute value circuit preceding the multiplier, as is the case with other methods.

The particular device chosen for the prototype was the AD533JD integrated circuit (shown in Fig. 2.3). This is not the cheapest four-quadrant multiplier on the market, but it has the advantage of being simple to operate, with the minimum of external components. The i.c. comprises a transconductance multiplying element, a stable reference, and an output operational amplifier on a single monolithic silicon chip.

The AD533JD multiplies with a transfer function of $\frac{XY}{10}$. The division by 10 should not worry the programmer but it should always be borne in mind when solving a problem. The op-amp output provides ±10V at 5mA, and is fully protected against short circuits to ground or either supply voltage. The inputs are fully protected against overvoltage transients.

The Overload Warning Circuit

The operation of the overload warning circuit is very simple. The output of every computing amplifier is sampled and compared with a positive and a negative reference voltage. If the amplifier output goes higher than the positive reference voltage, an l.e.d. is switched on, to indicate that the amplifier is saturating in the positive sense. Similarly, if the amplifier output falls below the negative reference voltage another l.e.d. is switched on to indicate saturation in the negative sense. The prototype uses ±11V as the reference voltages. An overload warning circuit is shown in Fig. 2.4. Only one pair of comparators and l.e.d.s are shown but ten pairs are necessary to serve the ten computing amplifiers. This circuit is arranged on a separate p.c.b. shown in Fig. 2.6 with the component overlay shown in Fig. 2.8.

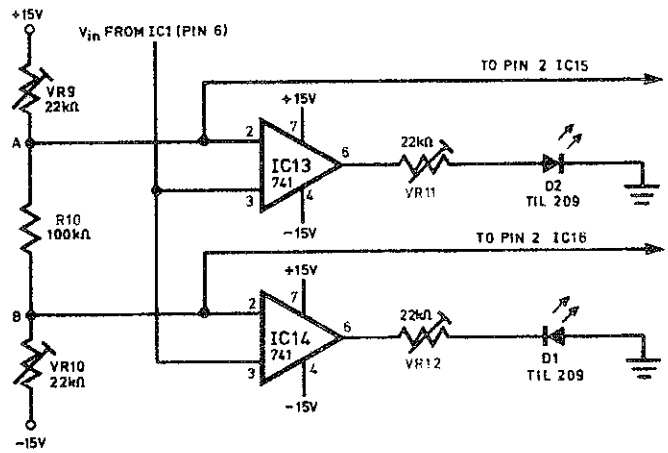


Fig. 2.4. Circuit diagram of the Overload Warning system required for each computing element

Resistor R9 and potentiometers VR11 and VR12 are connected across the positive and negative supply rails to form a potential divider that generates the positive and negative reference voltages of +11V and −11V. These voltages are applied to the inverting inputs of the twenty comparators as shown. The output of each computing amplifier is applied to the non-inverting inputs of the corresponding pair of comparators. The comparators drive the warning l.e.d.s, the brightness of which is set by preset potentiometers. The 741 op-amp was also used here as a comparator. Experience with the prototype has shown that the 741 is capable of driving the l.e.d.s with reasonable brightness without overheating.

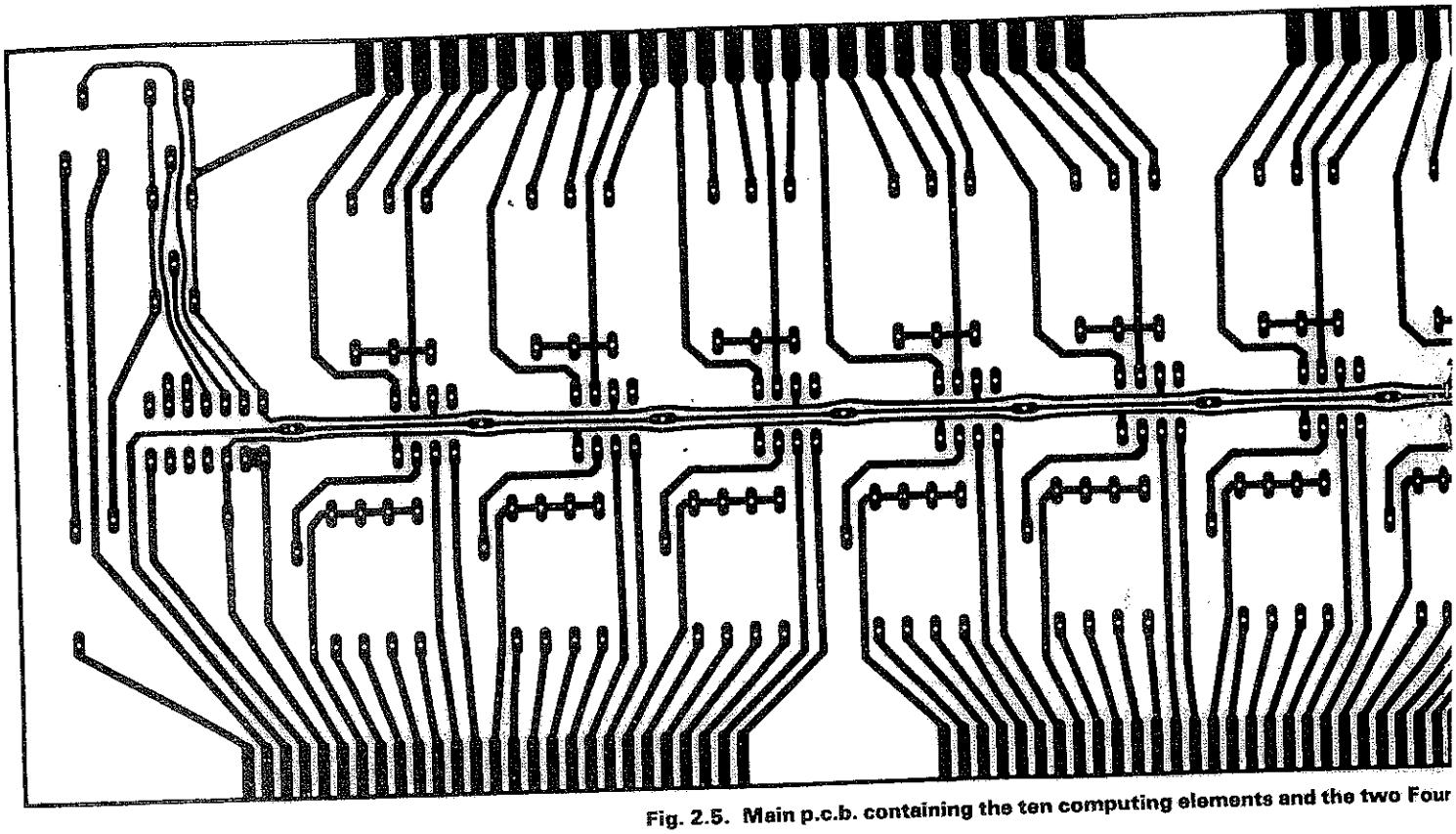


Fig. 2.5. Main p.c.b. containing the ten computing elements and the two Four

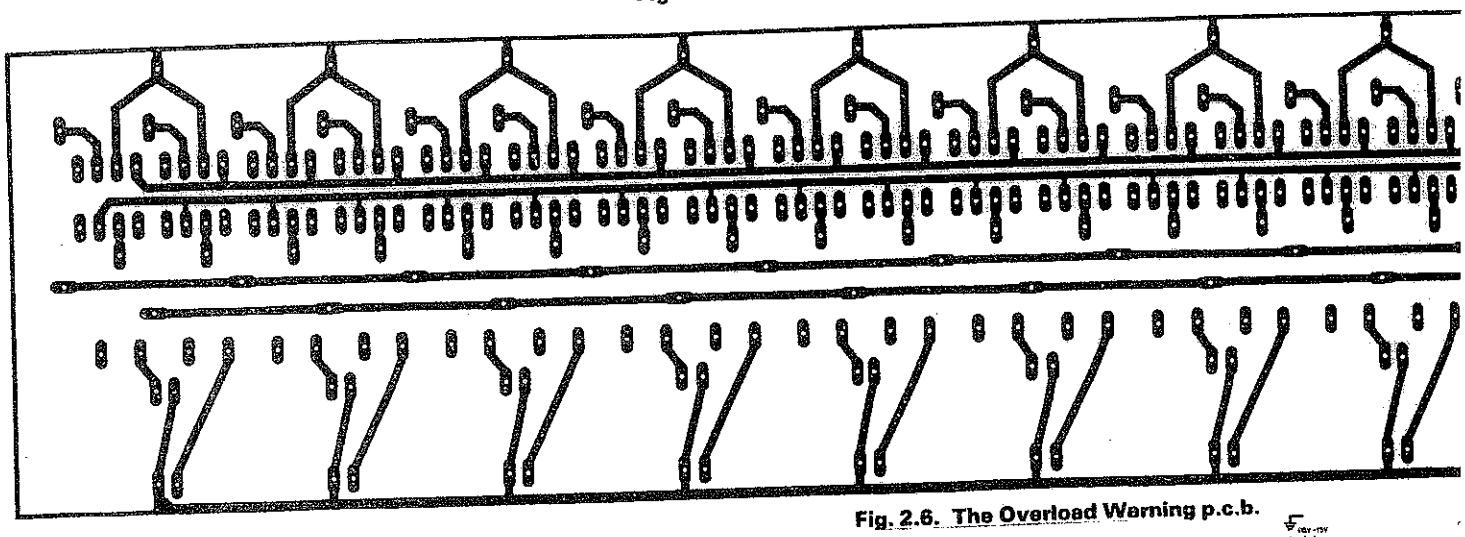
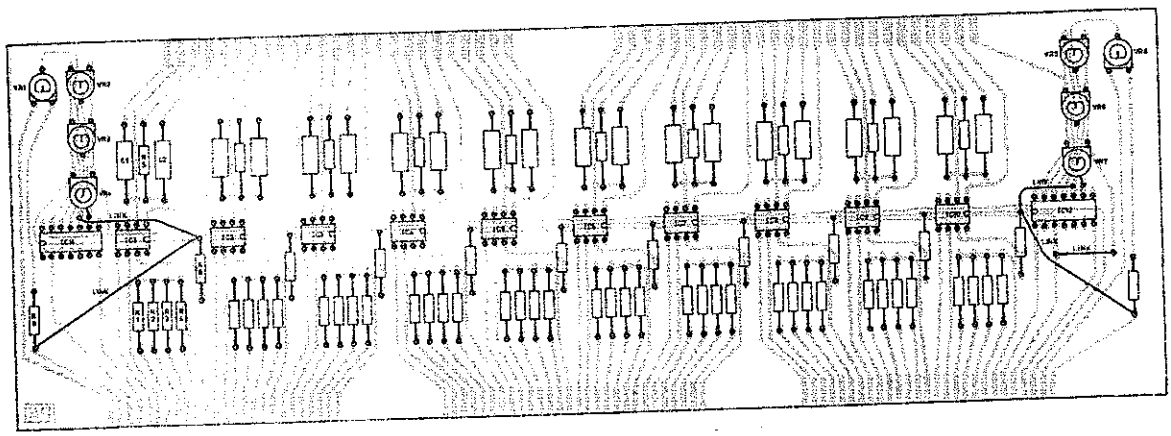


Fig. 2.6. The Overload Warning p.c.b.



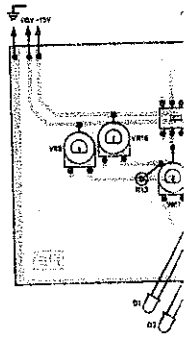
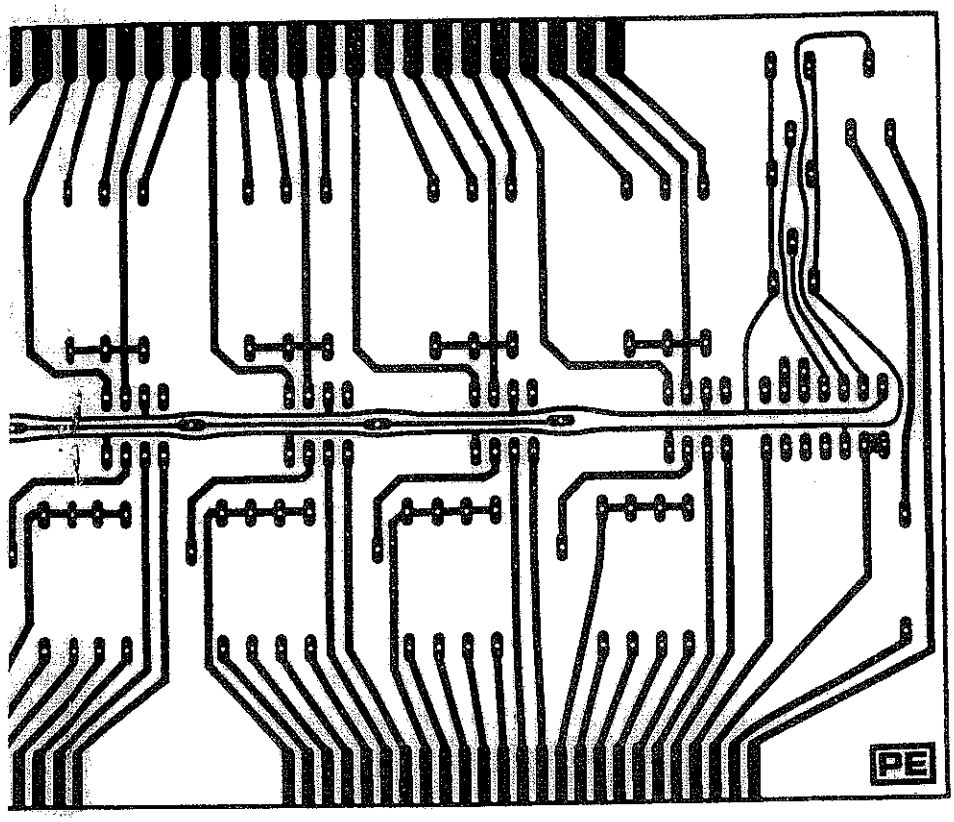
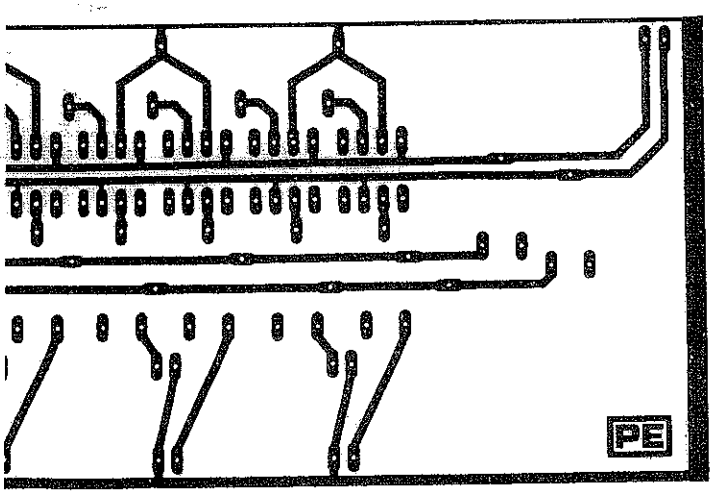


Fig. 2.7. Component layout for the main p.c.b.



o Four Quadrant Multipliers



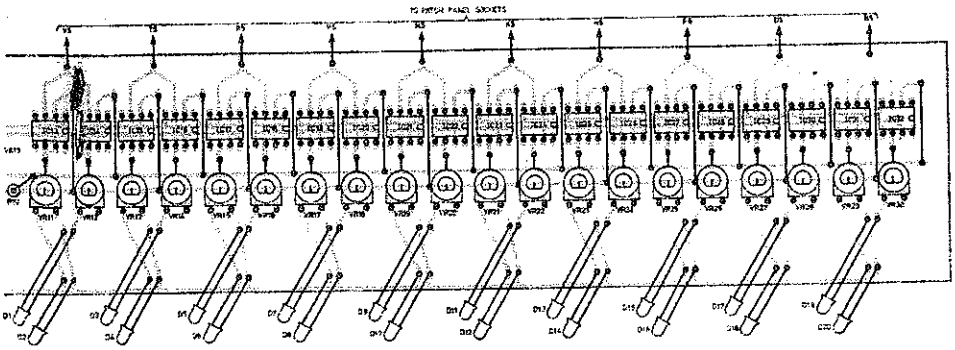


Fig. 2.8. Component layout for the Overload Warning Circuit

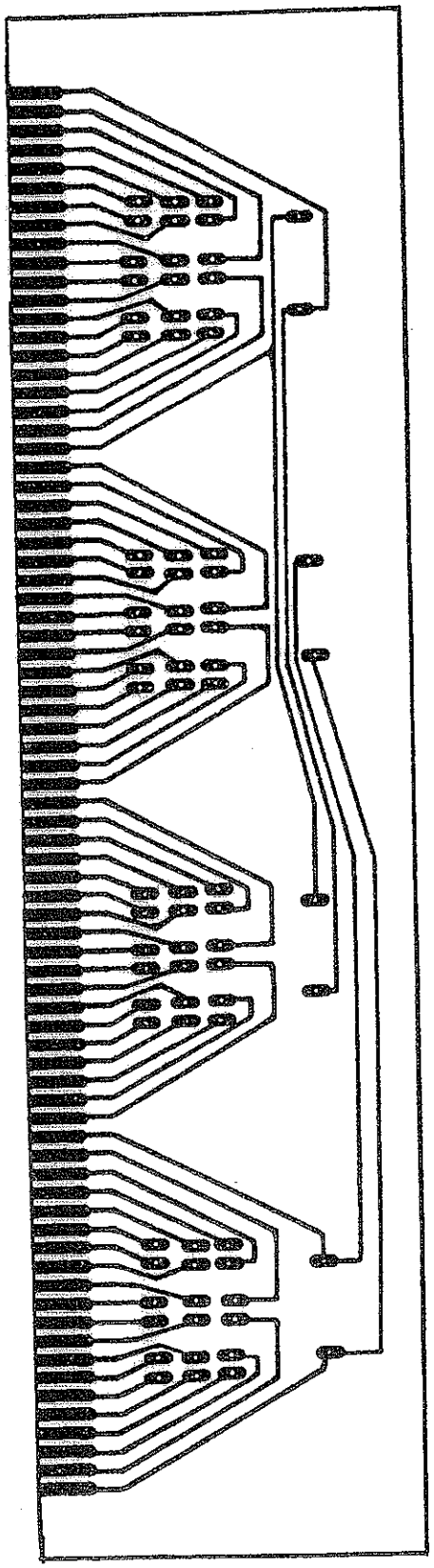
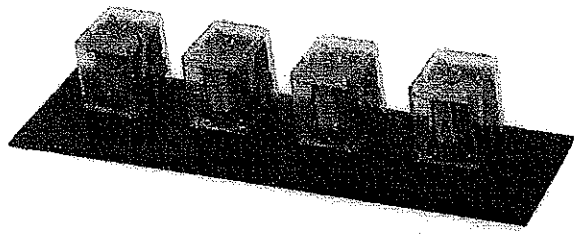
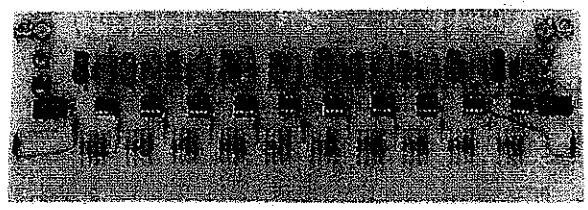


Fig. 2.9. P.c.b. design for the Relay Board





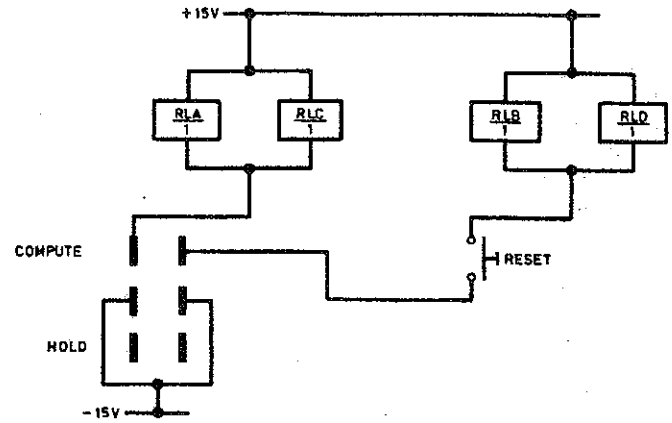


Fig. 2.11. Coil diagram for relays

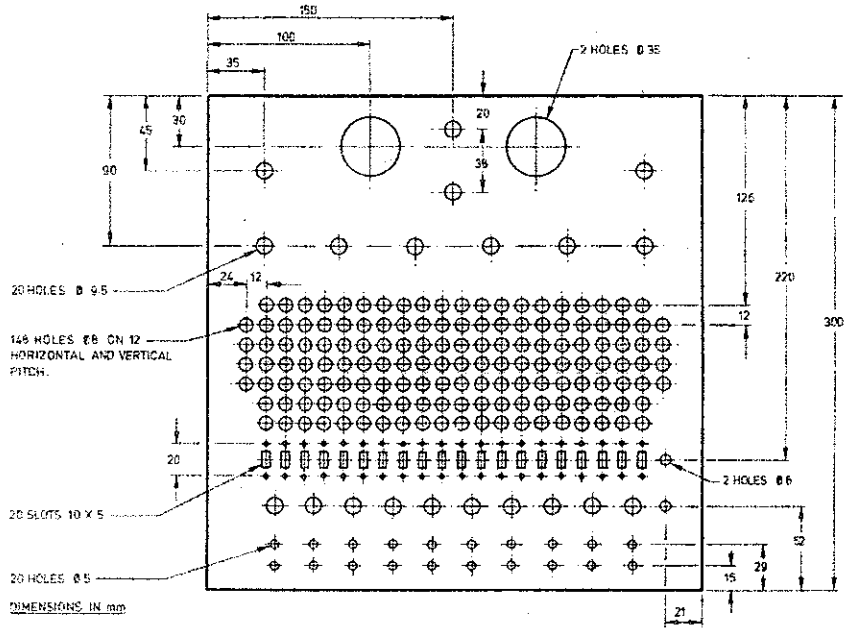
The Relay Mode Control P.C.B.

With ten amplifiers and two relay contacts per amplifier there is a need for twenty relay contacts. Complete mode control could be achieved with two ten-pole relays, one operating the RLA and C switches and the other the RLB and D switches. Ten-pole relays are difficult to find however and the prototype uses four six-pole relays operating in pairs. (The coil connections for the four relays are shown in Fig. 2.11.) This arrangement leaves four unused poles, which may become useful if it is decided to extend the computer.

The p.c.b. which accommodates the four relays is shown in Fig. 2.9. Connections to and from this board are also made via edge connectors.

Case Construction

The front panel requires a large surface area to accommodate the patch panel, potentiometers, switches, l.e.d.s etc. Because of this it will be difficult to obtain the right shaped case off the shelf. The prototype case was constructed from aluminium sheet. Two square panels form the front and the back of the case and the sides, top and bottom are cut and shaped as shown in Fig. 2.10, using the



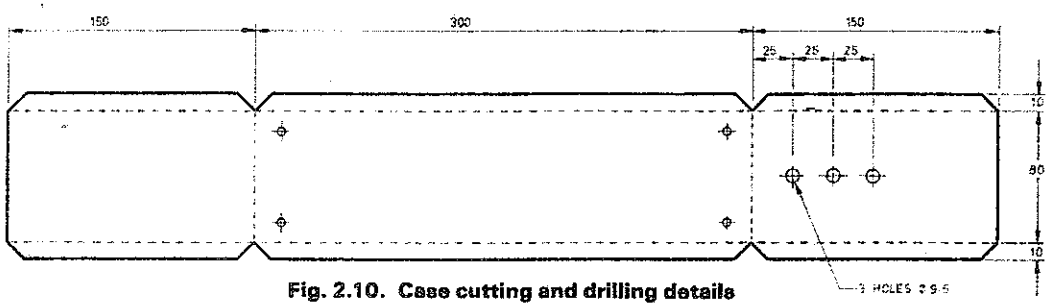
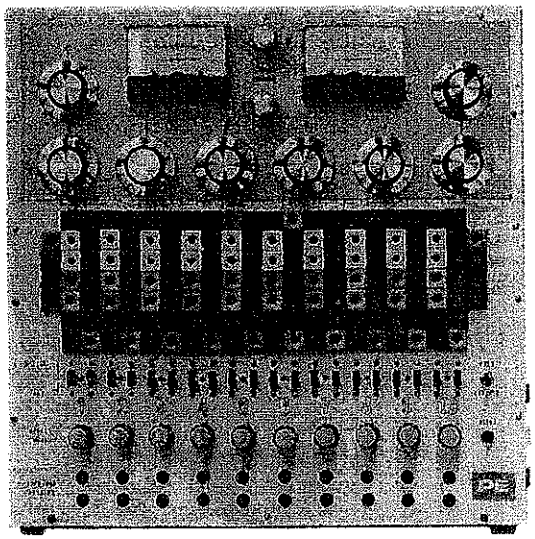


Fig. 2.10. Case cutting and drilling details

same gauge aluminium sheet. A bench vice, folding bar, and a sheet metal mallet are useful for this purpose. Fig. 2.10 shows the positions and dimensions of the holes required in the front panel. A lot of patience is required for the process of drilling, due to the large number of holes and the fact that a badly positioned hole will be detrimental to the appearance of the layout. This is particularly true in the case of the patch panel holes. A pitch of 12mm in both directions is enough to give a reasonable tolerance for positioning errors and at the same time avoid excessive gaps between the sockets. For the larger holes the use of sheet metal punches is recommended. Having drilled or punched all the holes, the front panel should then be labelled using dry letter transfers and sprayed with a clear lacquer fixative. The suggested labelling is shown in the photograph of the front panel.



The Patch Panel

The patch panel is constructed using 3·2mm sockets arranged in a matrix and packed together as closely as possible. There are 148 of these sockets and because identifying each one is difficult a colour coding system was used. Fig. 2.12 shows the arrangement of the sockets for one amplifier, one coefficient multiplier and one four-quadrant multiplier.

The pattern for the amplifier and coefficient multiplier shown in Fig. 2.12 is repeated ten times for the ten computing elements. The eight coefficient multipliers use 16 sockets on the top row. Two of the remaining four sockets are connected to the two panel meters and the other two are connected to batteries to provide reference voltages. Both positive and negative reference voltages will be needed for the solution of certain problems.

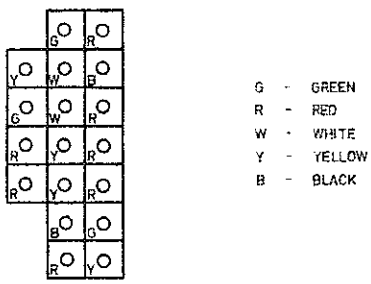


Fig. 2.12. Patch panel layout for one computing element (rows B and C) and one Four Quadrant Multiplier (row A)

For the four-quadrant multipliers four sockets are needed per multiplier and these are positioned on the extreme left and right of the patch panel.

COMPONENTS . . .

Resistors

R1, R2, R5	1MΩ ¼W 2% metal oxide (30 off)
R3, R4	100kΩ ¼W 2% metal oxide (20 off)
R8	270kΩ ¼W 5% carbon (10 off)
R9	100kΩ ¼W 5% carbon
R10	7·5kΩ ¼W 5% carbon (2 off)

Potentiometers

VR1, VR8	4·7kΩ (2 off)
VR2–VR7	22kΩ (6 off)
VR9–VR30	22kΩ (22 off)
VR31–VR40	10kΩ 0·5W Lin (10 off)

All horizontal min. presets except where stated

Capacitors

C1	1µF 160V (10 off)
C2	0·1µF 160V (10 off)

Semiconductors

IC1–IC30	741 op amp (30 off)
IC31–IC32	AD533JD (2 off)
D1–D20	TIL 209 (20 off)

Miscellaneous

4 off 6 way changeover relays
4 off mounting sockets for relays
holders for i.c.s (if req.)

CONSTRUCTOR'S NOTE: The AD533JD Four Quadrant Multiplier is available from **Analog Devices Ltd., Central Avenue, East Molesey, Surrey.**

Stage by Stage Construction

The computer has been designed so that it can be built in stages. At this point in the construction, ie, with the aluminium case and the p.c.b.s constructed and drilled, the constructor has to take a decision, as to whether he wants to opt for a stage construction. His choice can be very flexible. For example, one may decide that initially, all ten computing amplifiers are not absolutely necessary for the solution of simple problems with which the inexperienced programmer will be involved. Four amplifiers are enough to carry out fairly interesting experiments. Later, when more experience is gained, more computing amplifiers can be added as necessary. The same applies to the coefficient multipliers and the panel meters.

It should be mentioned that if four 6-pole relays are used for the mode control, as is the case with the prototype, at least two of these will be necessary even if only one or two amplifiers are used initially. Two 6-pole relays can provide mode control for six amplifiers.

Another area in which stage by stage construction can be applied, concerns the overload warning circuit. Here, the comparators and the l.e.d.s can be added following the addition of more amplifiers. Alternatively it may be decided to leave the warning circuit out altogether initially. This will make life difficult for the programmer, but it will not affect the operation of the computer.

NEXT MONTH: WIRING AND TESTING