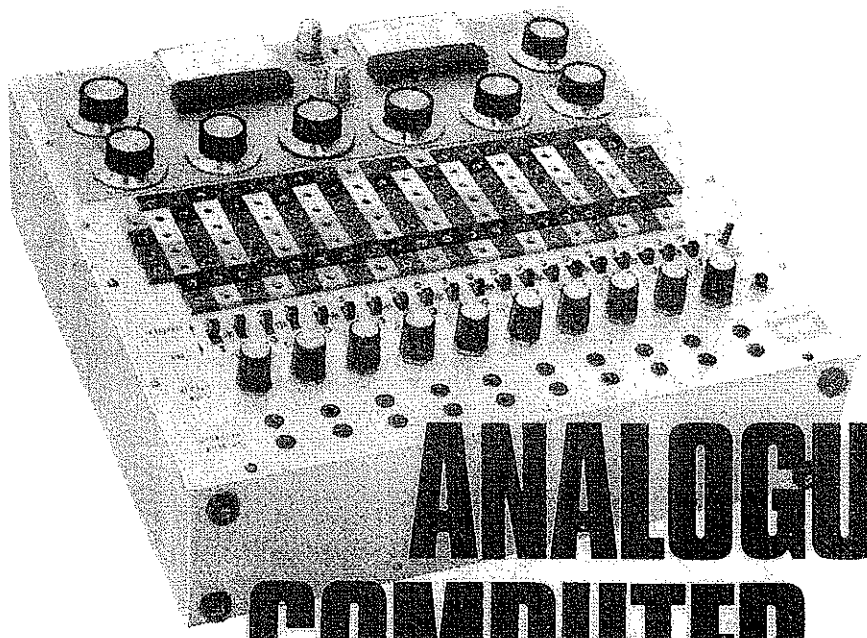


★ Wiring

★ Testing

★ Programming

ANALOGUE COMPUTER

P. J. KRONIS B.Sc.

PART 3

AFTER the p.c.b.s have been assembled and checked, all the components should be fitted into the case with the overload warning p.c.b. mounted on the base of the box using 6BA screws. With all the components mounted in the case the coefficient multipliers and the two panel meters should be wired first, following the wiring diagram shown in Fig. 3.1. Resistors R6, R7 and the links shown in Fig. 3.2 should be wired to each of the ten computing amplifiers. The wiring to the relay board and main p.c.b. is via eight edge connectors and to ease the problem of wiring these connectors a wiring schedule is given in Fig. 3.3. The numbering and layout arrangement of the patch panel and switches is given in Fig. 3.4.

The main p.c.b. is mounted above the patch panel and the relay board above the offset null potentiometers as shown in the photograph. After the computer wiring has been completed and checked a ±15V power supply should be connected to the unit and the following test procedures followed.

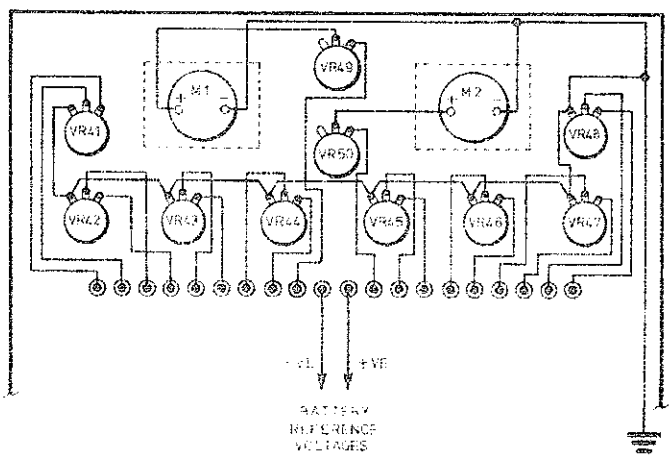
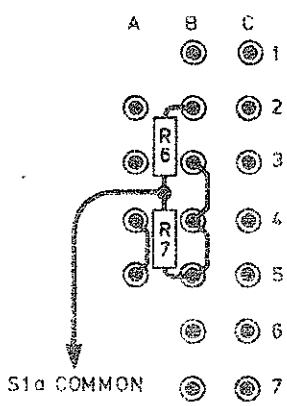


Fig. 3.1. Wiring diagram for the coefficient multipliers and panel meters

THE OFFSET NULL TRIM PROCEDURE

Set all the amplifiers to "add" by pushing all the slide switches down. Put the computer into the "compute" mode using the mode control switch and turn the sensitivity of the meters down as far as possible. Connect the output of the first amplifier (A1) to meter 1 (M1). Ground one of the x10 inputs of A1. This can be done by touching one end of the wire lead on the case. Connect the power supply and switch on. Increase the sensitivity of M1 gradually until the needle deflects to maximum if possible. Bring the needle back to zero by adjusting the offset null potentiometer of amplifier A1. Increase the sensitivity of the meter and repeat the same procedure until the needle is on zero when the meter is at maximum sensitivity.

Decrease the sensitivity fully and repeat the trim procedure for all amplifiers in the same way.



X and Y inputs
Common outputs
Coefficient multiplier input
Coefficient multiplier output
Initial conditions
Amplifier outputs
Amplifier inputs (X1)
Amplifier inputs (X10)
Spare socket
Integrate with nose gain of one
Integrate with nose gain of ten

Fig 3.2. Link wiring for amplifiers and multipliers

Edge Connector 1

From	To
pin 3	A3 Patch Panel
pin 4	Earth
pin 5	A2 Patch Panel
pin 6	−15V Supply
pin 7	A4 Patch Panel
pin 8	Edge Connector 6 pin 10
pin 9	C5 Patch Panel
pin 10	C4 Patch Panel
pin 11	C3 Patch Panel
pin 12	C2 Patch Panel
pin 13	TB1 Terminal Block
pin 14	VR51
pin 15	Edge Connector 6 pin 11
pin 16	E5 Patch Panel
pin 17	E4 Patch Panel
pin 18	E3 Patch Panel
pin 19	E2 Patch Panel
pin 20	TB2 Terminal Block
pin 21	VR52
pin 22	Edge Connector 6 pin 14
pin 23	G5 Patch Panel
pin 24	G4 Patch Panel
pin 25	G3 Patch Panel
pin 26	G2 Patch Panel
pin 27	TB3 Terminal Block
pin 28	VR53

Edge Connector 2

From	To
pin 1	Edge Connector 6 pin 15
pin 2	J5 Patch Panel
pin 3	J4 Patch Panel
pin 4	J3 Patch Panel
pin 5	J2 Patch Panel
pin 6	TB4 Terminal Block
pin 7	VR54
pin 8	Edge Connector 6 pin 18
pin 9	L5 Patch Panel
pin 10	L4 Patch Panel
pin 11	L3 Patch Panel
pin 12	L2 Patch Panel
pin 13	TB5 Terminal Block
pin 14	VR55
pin 15	Edge Connector 5 pin 19
pin 16	N5 Patch Panel
pin 17	N4 Patch Panel
pin 18	N3 Patch Panel
pin 19	N2 Patch Panel
pin 20	TB6 Terminal Block
pin 21	VR56
pin 22	Edge Connector 5 pin 20
pin 23	Q5 Patch Panel
pin 24	Q4 Patch Panel
pin 25	Q3 Patch Panel
pin 26	Q2 Patch Panel
pin 27	TB7 Terminal Block
pin 28	VR57

Edge Connector 3

From	To
pin 3	Edge Connector 5 pin 23
pin 4	S5 Patch Panel
pin 5	S4 Patch Panel
pin 6	S3 Patch Panel
pin 7	S2 Patch Panel
pin 8	TB8 Terminal Block
pin 9	VR58
pin 10	Edge Connector 5 pin 24
pin 11	U5 Patch Panel
pin 12	U4 Patch Panel
pin 13	U3 Patch Panel
pin 14	U2 Patch Panel
pin 15	TB9 Terminal Block
pin 16	VR59
pin 17	Edge Connector 5 pin 27
pin 18	W5 Patch Panel
pin 19	W4 Patch Panel
pin 20	W3 Patch Panel
pin 21	W2 Patch Panel
pin 22	TB10 Terminal Block
pin 23	VR60
pin 24	X2 Patch Panel
pin 25	X4 Patch Panel
pin 27	X3 Patch Panel

Edge Connector 4

From	To
pin 2	+15V Supply
pin 3	VR51
pin 4	B6 Patch Panel
pin 5	S1d Add
pin 6	B5 Patch Panel
pin 7	C6 Patch Panel
pin 8	VR52
pin 9	D6 Patch Panel
pin 10	S2d Add
pin 11	D5 Patch Panel
pin 12	E6 Patch Panel
pin 13	VR53
pin 14	F6 Patch Panel
pin 15	S3d Add
pin 16	F5 Patch Panel
pin 17	G6 Patch Panel
pin 18	VR54
pin 19	H6 Patch Panel
pin 20	S4d Add
pin 21	H5 Patch Panel
pin 22	J6 Patch Panel
pin 23	VR55
pin 24	K6 Patch Panel
pin 25	S5d Add
pin 26	K5 Patch Panel
pin 27	L6 Patch Panel

Edge Connector 5

From	To
pin 2	VR56
pin 3	M6 Patch Panel
pin 4	S6d Add
pin 5	M5 Patch Panel
pin 6	N6 Patch Panel
pin 7	VR57
pin 8	P6 Patch Panel
pin 9	S7d Add
pin 10	P5 Patch Panel
pin 11	Q6 Patch Panel
pin 12	VR58
pin 13	R6 Patch Panel
pin 14	S8d Add
pin 15	R5 Patch Panel
pin 16	S6 Patch Panel
pin 17	VR59
pin 18	T6 Patch Panel
pin 19	S9d Add
pin 20	T5 Patch Panel
pin 21	U6 Patch Panel
pin 22	VR60
pin 23	V6 Patch Panel
pin 24	S10d Add
pin 25	V5 Patch Panel
pin 26	W6 Patch Panel

Edge Connector 6

From	To
pin 3	−15V Supply
pin 4	S2c Common
pin 5	S1c Common
pin 9	TB1 Terminal Block
pin 10	S1b Add
pin 11	S2b Add
pin 12	TB2 Terminal Block
pin 13	TB3 Terminal Block
pin 14	S3b Add
pin 15	S4b Add
pin 16	TB4 Terminal Block
pin 17	TB5 Terminal Block
pin 18	S5b Add
pin 19	S5a Common
pin 20	S4c Common
pin 21	S3c Common
pin 22	S11a Compute
pin 23	TB2 Terminal Block
pin 24	TB1 Terminal Block
pin 28	Earth, Edge Connector 7 pin 3

Edge Connector 7

From	To
pin 1	S1a Integrate
pin 2	S2a Integrate
pin 3	Edge Connector 7 pin 4
pin 4	Edge Connector 7 pin 7
pin 5	S3a Integrate
pin 6	S4a Integrate
pin 7	Edge Connector 7 pin 8
pin 8	Edge Connector 8 pin 9
pin 9	S5a Integrate
pin 10	TB5 Terminal Block
pin 11	TB4 Terminal Block
pin 12	TB3 Terminal Block
pin 13	S7c Common
pin 14	S6c Common
pin 18	TB6 Terminal Block
pin 19	S6b Add
pin 20	S7b Add
pin 21	TB7 Terminal Block
pin 22	TB8 Terminal Block
pin 23	S8b Add
pin 24	S9b Add
pin 25	TB9 Terminal Block
pin 26	TB10 Terminal Block
pin 27	S10b Add
pin 28	S10c Common

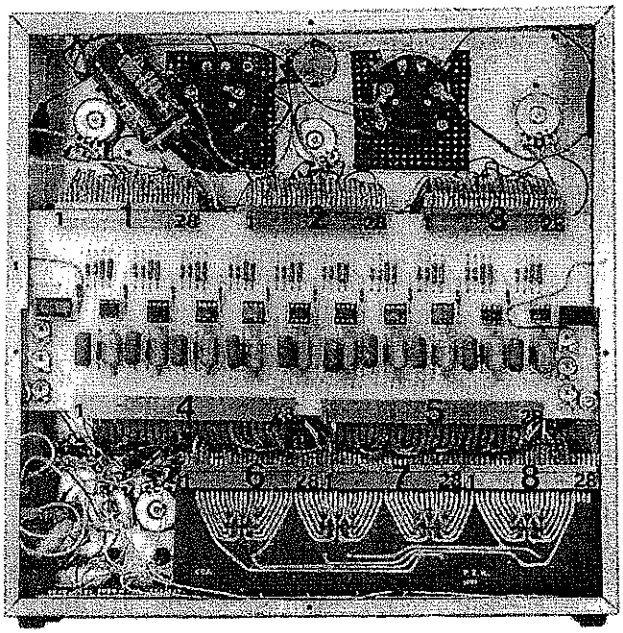
Edge Connector 8

From	To
pin 1	S9c Common
pin 2	S8c Common
pin 3	+15V Supply
pin 4	TB7 Terminal Block
pin 5	TB6 Terminal Block
pin 9	Edge Connector 8 pin 12
pin 10	S6c Integrate
pin 11	S7a Integrate
pin 12	Edge Connector 8 pin 13
pin 13	Edge Connector 8 pin 16
pin 14	S8a Integrate
pin 15	S9a Integrate
pin 16	Edge Connector 8 pin 17
pin 18	S10a Integrate
pin 19	TB10 Terminal Block
pin 20	TB9 Terminal Block
pin 21	TB8 Terminal Block
pin 22	Reset Switch (S12)

Fig. 3.3. Wiring Schedule

Wiring Schedule—*cont.*

From	To
S1b, S1d Common	TB1 Terminal Block
S2b, S2d Common	TB2 Terminal Block
S3b, S3d Common	TB3 Terminal Block
S4b,S4d Common	TB4 Terminal Block
S5b, S5d Common	TB5 Terminal Block
S6b, S6d Common	TB6 Terminal Block
S7b, S7d Common	TB7 Terminal Block
S8b, S8d Common	TB8 Terminal Block
S9b, S9d Common	TB9 Terminal Block
S10b, S10d Common	TB10 Terminal Block
Reset Button (S12)	S11b Compute
S11a	+15V Supply
S11b	−15V Supply
−15V Supply	VR51 Wiper
VR51 Wiper	VR52, 53, 54, 55, 56, 57, 58, 59, 60 (Wipers)



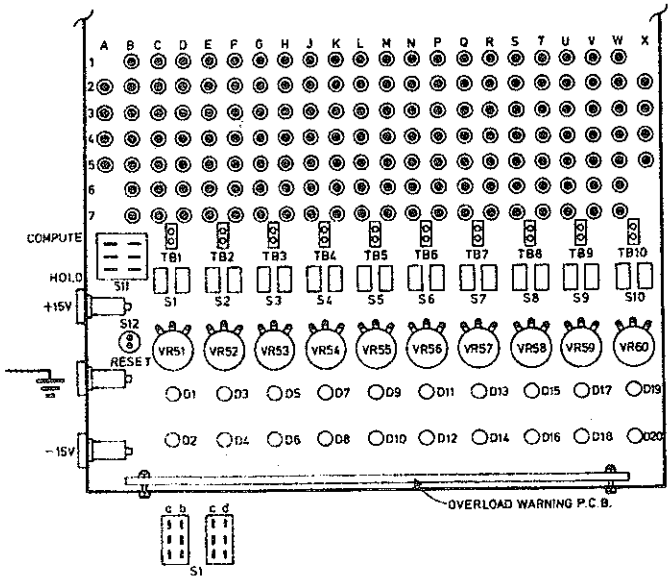


Fig. 3.4. Layout arrangements for edge connectors, patch panel and switches

MODE CONTROL TEST

Set amplifier A1 to "integrate", and the mode to "compute" and monitor the output with one of the meters. Apply a voltage to a ×1 input. The needle should deflect gradually in the positive direction, if the applied input voltage is negative, and vice-versa, until the amplifier saturates. When this happens, adjust the meter sensitivity so that the needle is at maximum deflection. Put the computer in the "hold" mode and press the "reset" switch. The needle should go to zero. Release "reset" and switch to "compute". The needle will again start to deflect and this time switch the mode to "hold" before the amplifier saturates. The needle should then stop moving. Carry out this test with all the amplifiers. While doing this, observe the operation of the overload warning circuit. The appropriate l.e.d. should come on when the amplifier output exceeds +11V or goes below −11V. Check both positive and negative operation by applying both positive and negative input voltages.

The above tests are not complete by any means but any remaining problems will show up when the examples described under "programming" are attempted.

COMPONENTS . . .

Resistors

R6, R7 100kΩ ¼W carbon (2 off)

Potentiometers

VR41–VR48 100 kΩ linear (8 off)
VR49–VR50 300 kΩ linear (2 off)

Miscellaneous

1 off d.p.d.t. switch (R.S. type 316–793)
20 off d.p.d.t. sub-min slide switch
2 off 50–0–50μA (ME15 T40 Watford Electronics)
1 off Push button (R.S. type 337–914)
151 off Square 4mm panel mounted sockets (55 red, 32 yellow, 22 green, 21 white, 21 black)
8 off Skirted knob
12 off Plain knob
6 off 28 way edge connector 0·1in matrix
2 off 28 way edge connector 0·15in matrix
Banana plugs (as required)

PROGRAMMING

It has already been mentioned, that it is necessary to form a mathematical model of the problem to be solved and the computer cannot help us to do this, but being very faithful however, it will happily try to solve a problem even if the wrong information is fed into it. Fortunately, in such cases the programmer could get an indication that something had gone wrong by studying the results which are usually meaningless. The general rule "Garbage In, Garbage Out" (well known to digital computer programmers) applies here also. Unfortunately, error checks cannot be incorporated in the analogue programs, as is the case with digital programs. It is important therefore to adopt a methodical procedure for programming to avoid errors.

Having formed the mathematical model, the equations are rearranged and a flow diagram is constructed which satisfies the equations. All values to be input and all computing elements to be used, are marked on the flow diagram to avoid confusion. Referring to the diagram the computer is then programmed by patching the panel. This procedure will be illustrated by several examples. The flow diagrams are constructed using standard symbols representing computing elements. Some of these have already been given. Fig. 3.5 shows all the symbols to be used in this article.

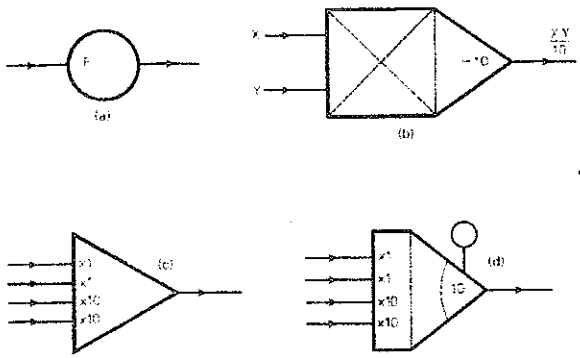


Fig. 3.5. Computing element symbols: (a) coefficient multiplier; (b) Four quadrant multiplier; (c) Summer; (d) Integrator with initial conditions.

As a first example let us examine the operation of potentiometers, adders and integrators, using simple experiments.

Apply a reference voltage to the input of P1 and connect the output to M1. Adjust the sensitivity of M1 so that when P1 is at maximum, M1 deflects fully. Operate the potentiometer and observe the results.

Switch the power on and calibrate M1 by applying a known voltage (e.g. supply voltage), to read 15V at full deflection. Switch A1 to "add" and apply the output of P1 to the input of A1 and the output of A1 to M1. The flow diagram and patch panel connections are shown in Fig. 3.6. Test all A1 inputs in turn and observe the gain of the adder each time.

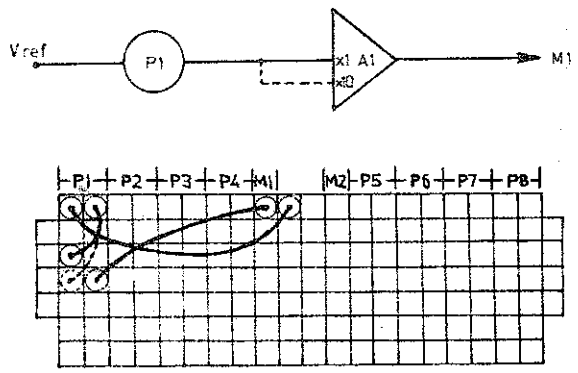
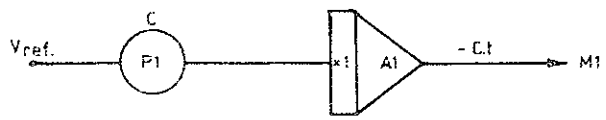


Fig. 3.6. Flow diagram and patch panel layout for the potentiometer example

To examine the operation of the integrators, we can integrate various functions and study the results. First let us see what happens when we integrate a constant, C. The mathematicians will immediately give us the answer as C.t + K, where t is the variable (time in this case) and K is another constant. This is a straight line, of gradient C and passing through the origin, if we have no initial conditions, i.e. C = 0 at t = 0. To verify this we can set up the program shown in Fig. 3.7.



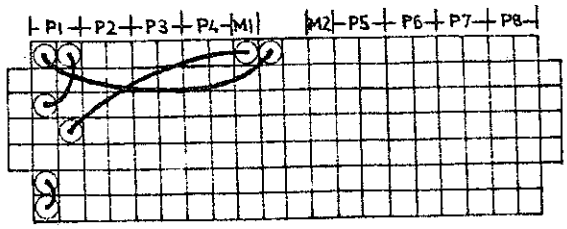


Fig. 3.7. Flow diagram and patch panel layout for the integration example

To run this program follow these steps:

(1) Check A1 is in "integrate"
(2) Computer mode: "hold"
(3) Switch power on
(4) Press reset for a few seconds and release
(5) Switch to "compute" and observe the meter.

Vary the value of C by adjusting P1 and repeat the above steps. If an X–Y plotter is available the results can be plotted for different values of C. The graph would look like Fig. 3.8. With C set to 1 volt the output should increase at 1 volt per second (C = C.t). This can be verified by timing the deflection of the needle.

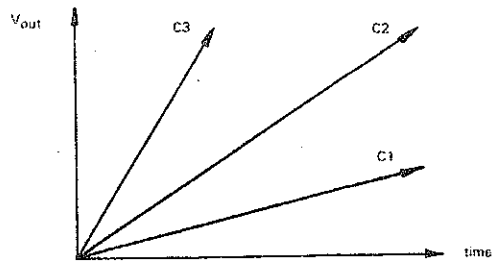


Fig. 3.8. Graph showing the resultant curves when various values for the constant C are integrated

These examples serve to illustrate the use of the analogue computer as a function generator. By integrating a step function we obtained a ramp function, the slope of which we could easily control. The ramp function can be integrated again to produce a square law function. This is shown in the flow diagram in Fig. 3.9. Still higher power functions can be obtained by successive integrations.

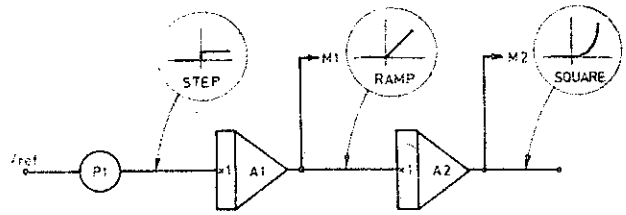


Fig. 3.9. By integrating waveforms the analogue computer can be used as a function generator

INITIAL CONDITIONS EXAMPLE

In the previous integrator examples we assumed that at time t = 0 all variables had zero value. Suppose that we wanted to give a value to the output of the integrator, before the computation begins. It is not difficult to imagine examples where this might be used. We may for example like to investigate the flight of a rocket, not from the point of launch but from some height above the launching pad, at which the rocket will have some velocity and acceleration. To illustrate the use of initial conditions we can repeat the first integrator example, but this time we are going to give an initial value to the integrator output of 5V. We therefore

require 5V to be applied to the initial condition socket of A1. Since the value of the reference voltages is only about 1·5V, we shall have to multiply this value. This we can do with the aid of an adder and a potentiometer. The flow diagram and patch panel connections are shown in Fig. 3.10.

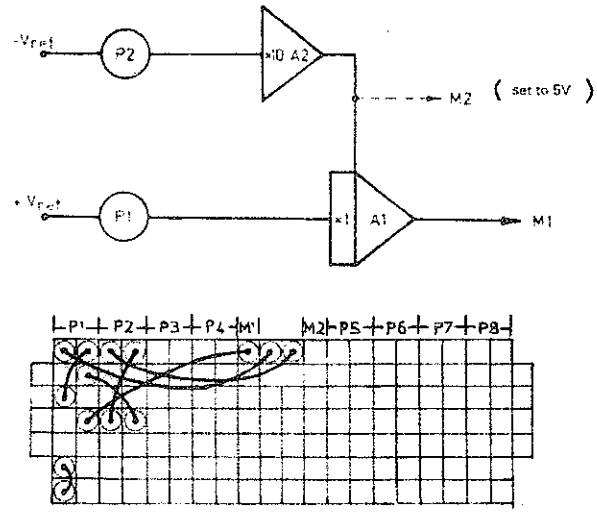


Fig. 3.10. Flow diagram and patch panel layout for the initial condition example

To run this program follow these steps after the panel has been patched.

(1) Switch power on
(2) Amplifier A1 integrating and A2 adding
(3) Computer mode: "hold"
(4) Monitor A2 output and adjust to 5V using P2
(5) Set output of P1 to 1V
(6) Press "reset" for a few seconds and release (Output of A1 should now show 5V)
(7) Switch mode to "compute" and observe M1.

The initial condition value is invariably formed using an adder and a potentiometer, unless of course the exact value is available. It is therefore common practice not to show these two computing elements, but simply to note the value being applied to the initial condition socket as shown in Fig. 3.11.

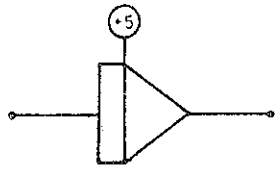


Fig. 3.11. Initial condition symbol

Another point worth noting here is that it is not essential for the potentiometer to precede the adder as shown in the flow diagram. In fact in such cases it is better for the amplifier to precede the potentiometer, as the former presents a higher input impedance to the battery than the latter and therefore saves battery energy.

ENGINEERING PROBLEMS

Consider a mass M supported on a spring of stiffness K. If the mass is disturbed, the system will begin to oscillate about the equilibrium position. Mechanical systems usually have electrical equivalents or vice-versa. The electrical equivalent to the spring mass system is the capacitor inductor series circuit. Both systems are shown in Fig 3.12.

The equation of motion of the spring mass system is $M\ddot{x} + K x = 0$. The electrical system is described by a similar

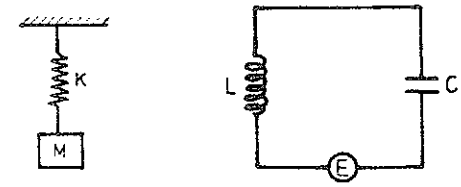


Fig. 3.12. The mechanical spring/mass circuit and its electrical equivalent the inductor/capacitor series circuit

equation but with electrical symbols substituted for the mechanical ones. The "dot" notation is used where time derivatives are involved. For example, one dot means the first derivative of the variable in question, with respect to time, two dots mean the second derivative and so on. So if x represents displacement, then $\dot{x}$ represents velocity, and $\ddot{x}$ acceleration. The equation can be rearranged so that the highest derivative appears on the left-hand side, with everything else on the right-hand side. This is normal practice when solving a problem on the analogue computer. The equation becomes $\ddot{x} = -\frac{K}{M} x$ and the flow diagram is shown in Fig. 3.13.

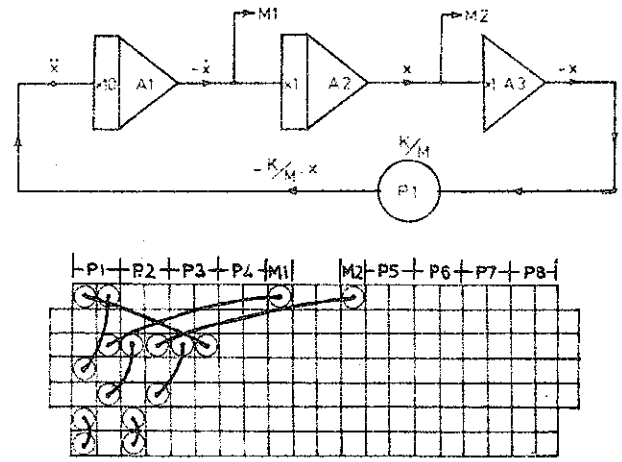


Fig. 3.13. Flow diagram and patch panel layout for the spring/mass example

By integrating $\ddot{x}$ twice we obtain $-\dot{x}$ and x. In our equation, however, we require −x and so A3 is used as a sign inverter. The value K/M is set up on potentiometer P1, the output of which becomes $-K/M \cdot x$. This is equal to $\ddot{x}$ and therefore we can close the loop by connecting the output of P1 back to the input of A1. The system as it stands will not vibrate unless it is disturbed. Theoretically once it is disturbed, it should go on vibrating for ever. In practice, however, we know that this is not true, because of the presence of some damping, due to air resistance in the case of the mechanical system and electrical resistance in the case of the electrical system. The analogue computer should produce results very near to the theoretical predictions, i.e. very little damping should be present. To run this program follow these steps.

(1) Check A1 and A2 are integrating and A3 is adding.
(2) Switch power on.
(3) Switch mode to "compute".
(4) Apply a disturbance to the input of A2 or A3. (This can be done by momentarily touching the input socket, with a wire lead connected to a reference voltage socket. This is equivalent to giving the weight a gentle push.)

(5) Observe the meters and adjust the sensitivity to produce a reasonable needle deflection.
(6) Operate P1 and see what happens to the frequency and amplitude of oscillation.

You should find that a high value of K/M (i.e. high spring stiffness or small mass or both) gives a high frequency and vice versa. The other point to note is that the oscillation is sinusoidal. The output of A1 (i.e. the velocity) is a cosine function, whereas that of A2 (the displacement) is a sine function. There is a phase difference of 90 degrees between the velocity and the displacement. (The mass comes to a momentary stop when the displacement is at a maximum.) This is shown in the graph in Fig 3.14.

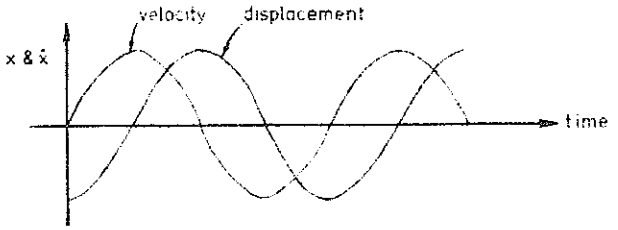


Fig. 3.14. Graph showing the phase difference between velocity and displacement

In this last example we have seen how the analogue computer can be used as a function generator for sine or cosine functions, with variable frequency. The frequency of oscillation is given by

$$f = \frac{1}{2\pi}\sqrt{\frac{K}{M}}\ \text{Hz (cycles per second)}$$

This can be checked by counting the number of cycles in one minute and dividing by 60 to convert to cycles per second. If the value of P1 is set to 1·0 and the input of A1 is multiplying by 10 then K/M = 10 and the frequency should be $f = 1/2\sqrt{10} = 0{\cdot}503$Hz.

NEXT MONTH: PROGRAMMING AND SPECIAL CIRCUITS (conclusion of series)

News Briefs

by Mike Abbott

BUBBLING WITH BITS

THE IDEA of the magnetic bubble conjures up a picture of quivering clusters gurgling their way to the North Pole. In fact powerful magnetic bubble memories are about to "pop" onto the scene from at least two major electronics manufacturers in the near future, one of which is Texas Instruments.

Sample quantities of a new quarter-million-bit bubble memory will be available from T.I. before the end of this year, but at $500 each there probably won't be many P.E. constructors in the queue. (A 92k—bit bubble memory is now in volume production at a price of $100 in 100 unit quantities). The big one however, designated the TIB0303, is full of three micron diameter magnetic bubble domains, and uses separate I/O, minor loop architecture, and features block replication of data. Separate read and write tracks with minor loop data storage are at the heart of this block replicate-based architecture to provide improved performance.

A total of 252 minor loops, each consisting of 1,137 bubble positions, results in a single-chip memory capacity of 286,524 bits. However, 224 loops are utilised resulting in a minimum data capacity of 254,688 bits.

Data bits are written into the write track and exchanged with stored data in the minor loops via swap gates. Data blocks are replicated simultaneously at minor loop and output track junctions, rather than serial duplication which is characteristic of major/minor loop architecture. Consequently, power-down cycle time is significantly reduced from 12·8 milliseconds in the 92K-bit major/minor loop configuration to 12·5 microseconds for block replicate, representing three orders of magnitude improvement.

Other key features include: advanced asymmetric chevron design for improved bubble propagation and transfer, merged data that allows a continuous flow of data bits at the read track, and a dedicated loop for storage of on-chip redundancy information and address synchronisation.

Performance specifications at 100 kilohertz operation are an average access time of 7·3 milliseconds for the first bit of the 224-bit page and a typical power consumption of 0·9 watt for continuous operation. A data-merge function allows a read data of 100K bits per second. Operating temperature is 0° to 50°C with non-volatile storage range of −40° to 85°C.

Bubble control functions are executed by providing current pulses through the appropriate control element on the chip.

The bubble chip is comprised of a gadolinium-gallium garnet substrate upon which a magnetic epitaxial film is grown. Patterns of permalloy metal are deposited on the epitaxial film to define the path of the bubble domains in the presence of a rotating magnetic field. As the field rotates, the bubble domains move under the permalloy pattern in shift register fashion.

The TIB0303 will be offered in a 20-pin dual-in-line package, measuring 30 × 30 × 10mm. The package contains the quarter-million-bit bubble chip surrounded by two orthogonal coils that provide the rotating magnetic field, a permanent magnet set, and a magnetic shield to protect data from external fields.

Taking a systems approach, TI will offer a family of interface and control circuits for the TIB0303 in the second quarter of 1979.

BLINKING GOOD

IF ONE of your projects requires an l.e.d. to wink on-and-off to catch someone's eye, here's something to save you the effort of building a multivibrator to do it.

Available from the Norbain Optoelectronics Division is the first Flashing Light Emitting Diode, Type FRL 4403, to appear on the market. The T 1¾ l.e.d. is manufactured in Gallium Arsenide Phosphide technology with a red diffused plastic lens. The built-in integrated circuit flashes the l.e.d. on and off at roughly 3 pulses per second, and can be driven directly by standard TTL and CMOS devices, eliminating the need for external switching circuitry.

Optoelectronic characteristics include a luminous intensity of 1·2mCd (typ), an emission peak wavelength of 650nm, spectral line half width 40nm, operating voltage 5 volts (typ), and current of 20 milliamps (typ).

The l.e.d. gives a large full flood radiating area, wide viewing angle and finds application as a condition warning light, monitoring process control system and in many other applications where warning of failure is essential.

Norbain Optoelectronics Division, Norbain House, Arkwright Road, Reading, Berkshire RG2 0LT.

ON THE LEVELL

THE very popular and stout a.c. microvolt meters, type TM3B, made by Levell Electronics Ltd., have just been upgraded.

The improvements include increased input impedance and meter scale length. A brief specification follows:

VOLTAGE and dB RANGES: 15μV to 500V. f.s.d. Acc. ±1% f.s.d. ±1μV at 1kHz, −100, −90 . . . +50dB. Scale −20dB/+6dB ref. 1mW/600Ω.

RESPONSE: ±3dB from 1Hz to 3MHz, ±0·3dB from 4Hz to 1MHz above 500μV.

INPUT IMPEDANCE: Above 50mV: 10MΩ<20pf. On 50μV to 50mV: >5MΩ<50pf.